



Attorney Docket No.: PROG2000-1C3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: <i>King</i>)	Art Unit: 2815
)	
Serial No.: <i>10/760,090</i>)	
)	Examiner: <i>Unassigned</i>
Filed: <i>01/15/04 as continuation of 10/315,741, filed</i>)	
<i>12/10/20, now U.S. patent no 6,686,631</i>)	
)	
For: <i>CMOS process compatible, tunable negative</i>)	
<i>differential resistance (NDR) device and method of</i>)	
<i>operating same</i>)	
)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

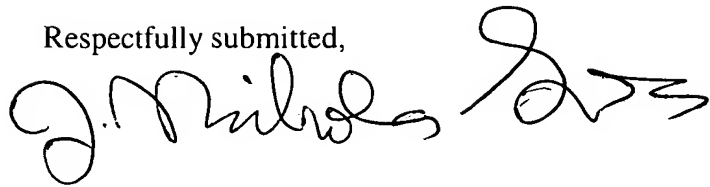
Sir:

1. Pursuant to 37 C.F.R. 1.97 and 1.98, and in compliance with 37 C.F.R. 1.56, the Office's attention is directed to the patents, publications and other information listed on the attached PTO-1449. Regarding the document(s), publication(s) or other information listed on the attached PTO-1449, Applicant believes the same may qualify as "prior" art to this application and should be treated accordingly, although Applicant(s) reserve(s) the right to contest the prior art status of any document, publication or information cited herein.

2. Pursuant to 37 C.F.R. 1.97(b) this Statement is being filed before the mailing date of a first Office action on the merits.

3. Copies of the aforementioned references were provided by the applicant and/or cited by the examiner in the related parent application to the above. Should it be necessary for the applicant to provide additional copies of any other references, please contact the undersigned.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "J. Nicholas Gross", followed by a stylized flourish or set of initials.

J. Nicholas Gross
Registration No. 34,175
Attorney for Applicant(s)

April 23, 2004
726 Duboce Ave.
San Francisco, CA 94117
Tel. (415) 355-9800
Fax (415) 355-9006

I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, this 23rd day of April 2004.



Information Disclosure Statement By Applicant

Substitute for form 1449/PTO

Page 1 of 5

Application Number: 10/760,090

Filing Date: 01/15/2004

First Named Inventor: King

Art Unit: 2815

Examiner Name: N/A

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Examiner Initials	Patent Number	Publication Date	Inventor Name
	US3588736	06/28/1971	Mcgroddy
	US4047974	09/13/1977	Harari
	US4143393	03/06/1979	DiMaria et al.
	US4219829	08/26/1980	Dorda et al.
	US4806998	02/21/1989	Vinter et al.
	US4945393	07/31/1990	Beltram et al.
	US5021841	06/04/1991	Leburton et al.
	US5032891	07/16/1991	Takagi et al.
	US5093699	03/03/1992	Weichold et al.
	US5130763	07/14/1992	Delhay et al.
	US5162880	11/10/1992	Hazama et al.
	US5189499	02/23/1993	Izumi et al.
	US5357134	10/18/1994	Shimoji
	US5390145	02/14/1995	Nakasha et al.
	US5477169	12/19/1995	Shen et al.
	US5543652	08/06/1996	Ikeda et al.
	US5606177	02/25/1997	Wallace et al.
	US5633178	05/27/1997	Kalnitsky
	US5689458	11/18/1997	Kuriyama
	US5698997	12/16/1997	Williamson et al.
	US5705827	01/06/1998	Baba et al.
	US5770958	06/23/1998	Arai et al.
	US5773996	06/30/1998	Takao
	US5804475	09/08/1998	Meyer et al.
	US5869845	02/09/1999	Van der Wagt et al.
	US5883549	03/16/1999	De Los Santos
	US5883829	03/16/1999	Van der Wagt
	US5895934	04/20/1999	Harvey et al.
	US5903170	05/11/1999	Kulkarni et al.
	US5907159	05/25/1999	Roh et al.
	US5936265	08/10/1999	Koga
	US5953249	09/14/1999	Van der Wagt
	US5959328	09/28/1999	Krautschneider et al.
	US5962864	10/05/1999	Leadbeater et al.
	US6015978	01/18/2000	Yuki et al.
	US6077760	06/20/2000	Fang et al.
	US6091077	07/18/2000	Morita et al.
	US6104631	08/15/2000	El-Sharawy et al.

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Page 2 of 5

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	US6246606	06/12/2001	Forbes et al.
	US6294412	09/25/2001	Krivokapic
	US6301147	10/09/2001	El-Sharawy et al.
	US6303942	10/16/2001	Farmer
	US Publication Number		
	2001/0005327	6/2001	Duane et al.
	2001/0019137	9/2001	Koga et al.
	Foreign Patent Number		
	EP 0526897 B1	8/1992	Baba
	EP 1085656 A2	9/1999	Den
	EP 1107317 A1	6/2001	Nakazato
	WO 9963598	12/1999	Nemati et al.
	WO 0041309	7/2000	Broekaert

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Substitute for form 1449/PTO

Page 3 of 5

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Examiner Initials	Non Patent References
	A. Seabaugh, "Promise of Tunnel Diode Integrated Circuits," Tunnel Diode and CMOS/HBT Integration Workshop, Dec. 9, 1999, Naval Research Laboratory, Washington, DC., 13 Pages.
	Jian Fu Zhang, "Traps: Detrapping," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: Dec. 27, 1999, John Wiley & Sons, Inc., 4 Pages.
	Jian Fu Zhang, "Traps: Effects of Traps and Trapped Charges on Device Performance," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: Dec. 27, 1999, John Wiley & Sons, Inc., 2 Pages.
	Jian Fu Zhang, "Traps: Measurement Techniques," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: Dec. 27, 1999, John Wiley & Sons, Inc., 5 Pages.
	Jian Fu Zhang, "Traps," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: Dec. 27, 1999, John Wiley & Sons, Inc., 2 Pages.
	Jian Fu Zhang, "Traps: Trapping Kinetics," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: Dec. 27, 1999, John Wiley & Sons, Inc., 2 Pages.
	Jian Fu Zhang, "Traps: Origin of Traps," Wiley Encyclopedia of Electrical and Electronics Engineering Online, Article Posting Date: Dec. 27, 1999, John Wiley & Sons, Inc., 4 pages.
	Seabaugh A., Brar B., Broekaert T., Morris F., and Frazier, G., "Resonant Tunneling Mixed Signal Circuit Technology," Solid-State Electronics 43:1355-1365, 1999, (11 pages).
	Farid Nemati et al., "A Novel High Density, Low Voltage SRAM Cell With a Vertical NDR Device," Center for Integrated Systems, Stanford University, CA (2 pages).
	Farid Nemati et al., "A Novel Thyristor-based SRAM Cell (T-RAM) for High-Speed, Low-Voltage, Giga-scale Memories," Center for Integrated Systems, Stanford University, CA, (4 pages).
	Shoucair F. et al., "Analysis and Simulation of Simple Transistor Structures Exhibiting Negative Differential Resistance," EECS Department, UC Berkeley, Berkeley, CA, (4 pages).
	Jungel, A, Pohl, C., "Numerical Simulation of Semiconductor Devices: Energy-Transport and Quantum Hydrodynamic Modeling," Fachbereich Math., Tech. Univ. Berlin, Germany, pp. 1-9, 1998.
	S.M.A. Nimour, R. Ouasti, N. Zekri, "Effect of Spatially Disordered Barriers on the Band Structure of Finite Superlattices," phys. stat. sol. (b) 1998, 209, No. 2, 311-318. (8 pages).
	C. Pacha, et al., "Resonant Tunneling Device Logic Circuits," Microelectronics Advanced Research Initiative (MEL-ARI), Jul. 1998-Jul. 1999, pp. 1-22.
	Gardner, Carl, Ringhofer, Christian, "Smooth Quantum Hydrodynamic Model Simulation of the Resonant Tunneling Diode," Dept. Of Mathematics Arizona State University, pp. 1-5, (1998).
	Serge Luryi and Mark Pinto, "Collector-Controlled States in Charge Injection Transistors," SPIE--92 Symposium, pp. 1-12, (1992).

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Page 4 of 5

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	Serge Luryi and Mark Pinto, "Collector-Controlled States and the Formation of Hot Electron Domains in Real-Space Transfer Transistors," AT & T Bell Laboratories, pp. 1-7, (1992).
	S. Luryi and M. Mastrapasqua, "Light-emitting Logic Devices based on Real Space Transfer in Complementary InGaAs/InAlAs Heterostructures", in "Negative Differential Resistance and Instabilities in 2D Semiconductors", ed. by N. Balkan, B. K. Ridley, and A. J. Vickers, NATO ASI Series [Physics] B307, pp. 53-82, Plenum Press (New York 1993).
	Shao, Z., Porod, W., Lent, C., & Kirkner, D., "Transmission Zero Engineering in Lateral Double-Barrier Resonant Tunneling Devices," Dept. of Electrical Engineering, University of Notre Dame, pp. 1-7 (1996).
	C. Pacha and K. Goser, "Design of Arithmetic Circuits using Resonant Tunneling Diodes and Threshold Logic," Lehrstuhl Bauelemente der Elektrotechnik, Universitat Dortmund, pp. 1-11, Sep. 1997.
	S. Mohan, et al., "Ultrafast Pipelined Adders Using Resonant Tunneling Transistors," IEE Electronics Letters, vol. 27, No. 10, May 1991, pp. 830-831. (2 pages)
	O. Le Neel, et al., "Electrical Transient Study of Negative Resistance in SOI MOS Transistors", Electronics Letters, vol. 26, No. 1, pp. 73-74, Jan. 1990.
	P. S. Barlow, et al., "Negative differential output conductance of self-heated power MOSFETs", IEE Proceedings--I Solid-State and Electron Devices, vol. 133, Part I, No. 5, Oct. 1986, pp. 177-179. (3 pages).
	E. Chan, et al., "Mask Programmable Multi-Valued Logic Gate Arrays Using RTDs and HBTs," IEE Proceedings--E: Computers and Digital Techniques, vol. 143, No. 5, Oct. 1996, pp. 289-294. (6 pages).
	E. Chan, et al., "Compact Multiple-Valued Multiplexers Using Negative Differential Resistance Devices," IEEE Journal of Solid-State Circuits, vol. 31, No. 8, Aug. 1996, pp. 1151-1156. (6 pages).
	S. Mohan, et al., "Ultrafast Pipelined Arithmetic Using Quantum Electronic Devices," IEE Proceedings--E: Computers and Digital Techniques, vol. 141, No. 2, Mar. 1994, pp. 104-110. (7 pages).
	S. Mohan, et al., "Logic Design Based on Negative Differential Resistance Characteristics of Quantum Electronic Devices," IEE Proceedings--G: Electronic Devices, vol. 140, No. 6, Dec. 1993, pp. 383-391. (9 pages).
	R. Oberhuber, et al., "Tunnel-Devices with Negative Differential Resistivity Based on Silicon?," Source: Deutsche Forschungsgemeinschaft and Siemens AG, date unknown, 2 pages.
	J. P. A. Van Der Wagt, et al., "RTD/HFET Low Standby Power SRAM Gain Cell," Source: Corporate Research Laboratories, Texas Instruments, 1998, 4 pages.
	G. I. Haddad et al., "Tunneling Devices and Applications in High Functionality/ Speed Digital Circuits," Solid State Electronics, vol. 41, No. 10, Oct. 1997, pp. 1515-1524. (10 pages).
	S. J. Koester, et al., "Negative Differential Conductance in Lateral Double-Barrier Transistors Fabricated in Strained Si Quantum Wells," Applied Physics Letters, vol. 70, No. 18, May, 1997, pp. 2422-2424. (3 pages).

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Page 5 of 5

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	S. L. Rommel, et al., "Room Temperature Operation of Epitaxially Grown Si/Si _{0.5} Ge _{0.5} /Si Resonant Interband Tunneling Diodes," Applied Physics Letters, vol. 73, No. 15, pp. 2191-2193, 1998. (3 pages).
	News Release from www.eurekalert.org/releases/udel-udcnflb.html , "UD Computer News: Future Looks Bright for Tunnel Diodes, Promising Faster, More Efficient Circuits," Oct. 1, 1998, 4 pages.
	P. Mazumder, et al., "Digital Circuit Applications of Resonant Tunneling Devices," Proceedings of the IEEE, vol. 86, No. 4, pp. 664-686, Apr., 1998. (23 pages).
	J. P. Sun, et al., "Resonant Tunneling Diodes: Models and Properties," Proceedings of the IEEE, vol. 86, No. 4, Apr. 1998, pp. 641-661. (21 pages).
	Alejandro F. Gonzalez, et al., "Standard CMOS Implementation of a Multiple-Valued Logic Signed-Digit Adder Based on Negative Differential-Resistance Devices," Proceedings of the 30th IEEE International Symposium on Multiple-Valued Logic (ISMVL 2000), 6 pages.
	G. Wirth, et al., "Negative Differential Resistance in Ultrashort Bulk MOSFETs," IECON'99 Conference Proceedings, vol. 1, San Jose, 1999, S. 29-34.
	R. H. Mathews, et al., "A New RTD-FET Logic Family," Proceedings of the IEEE, vol. 87, No. 4, pp. 596-605, 1999. (10 pages).
	J. P. A. Van Der Wagt, "Tunneling-Based SRAM," Proceedings of the IEEE, vol. 87, No. 4, pp. 571-595, 1999. (25 pages).
	C. P. Heij, et al., "Negative Differential Resistance Due to Single-Electron Switching," Applied Physics Letters, vol. 74, No. 7, Feb. 15, 1999, 5 pages.

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